+300°C

signetics

LINEAR INTEGRATED CIRCUITS

DESCRIPTION

The NE/SE 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA or drive TTL circuits.

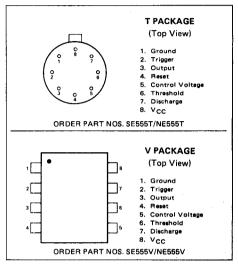
FEATURES

- TIMING FROM MICROSECONDS THROUGH HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- ADJUSTABLE DUTY CYCLE
- HIGH CURRENT OUTPUT CAN SOURCE OR SINK 200mA
- . OUTPUT CAN DRIVE TTL
- TEMPERATURE STABILITY OF 0.005% PER OC
- NORMALLY ON AND NORMALLY OFF OUTPUT

APPLICATIONS

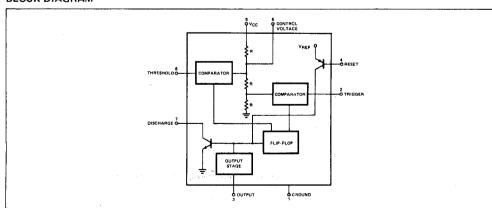
PRECISION TIMING
PULSE GENERATION
SEQUENTIAL TIMING
TIME DELAY GENERATION
PULSE WIDTH MODULATION
PULSE POSITION MODULATION
MISSING PULSE DETECTOR

PIN CONFIGURATIONS



Lead Temperature (Soldering, 60 seconds)

BLOCK DIAGRAM



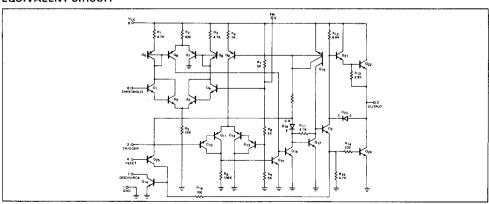
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified)

PARAMETER	TEST CONDITIONS		SE 555			NE 555		
		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V _{CC} = 5V R _I = 00		3	5		3	6	mA
	V _{CC} = 15V R ₁ = 00		10	12		10	15	mA
	Low State, Note 1							
Timing Error	R _A , R _B = 1KΩ to 100KΩ							
Initial Accuracy	C = 0.1 µF Note 2	1	0.5	2		1		%
Drift with Temperature			30	100		50		ppm/ ^O C
Drift with Supply Voltage			0.005	0.02	İ	0.01		%/Volt
Threshold Voltage			2/3			2/3		x v _{cc}
Trigger Voltage	V _{CC} = 15V	4.8	5	5.2	}	5		v
	V _{CC} = 5V	1.45	1.67	1.9	1	1.67		V
Trigger Current			0.5	1		0.5	i	μА
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	v
Reset Current			0.1			0.1		mA
Threshold Current	Note 3		0.1	.25		0.1	.25	μA
Control Voltage Level	V _{CC} = 15V	9.6	10	10.4	9.0	10	11	V
	V _{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage Drop (low)	V _{CC} = 15V				1			
	ISINK = 10mA		0.1	0.15		0.1	.25	V
	ISINK = 50mA		0.4	0.5		0.4	.75	٧
	ISINK = 100mA		2.0	2.2	1	2.0	2.5	V
	ISINK = 200mA	-	2.5	İ		2.5		
	V _{CC} = 5V		1					
	ISINK = 8mA		0.1	0.25				V
	ISINK = 5mA		1		1	.25	.35	
Output Voltage Drop (high)								
	ISOURCE = 200mA		12.5			12.5		
	V _{CC} = 15V	1						
	ISOURCE = 100mA							
	V _{CC} = 15V	13.0	13.3	l	12.75	13.3		٧
	V _{CC} = 5V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		nsec
Fall Time of Output			100	l		100		nsec

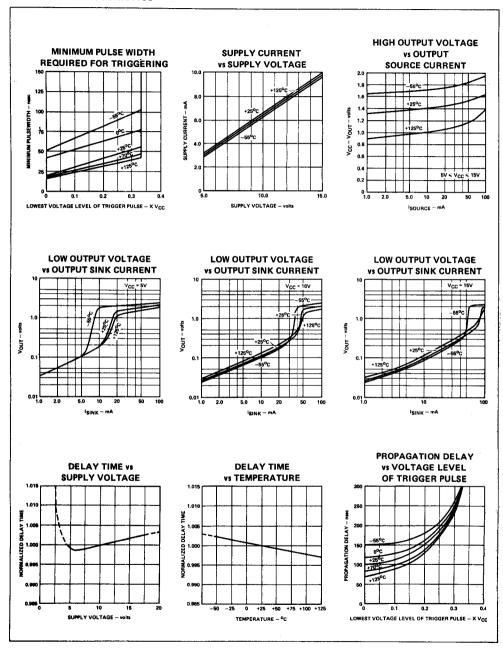
NOTES:

- 1. Supply Current when output high typically 1mA less.
- 2. Tested at V_{CC} = 5V and V_{CC} = 15V
- 3. This will determine the maximum value of R_A + R_B for 15V operation. The max total R = 20 megohm.

EQUIVALENT CIRCUIT

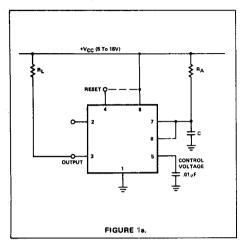


TYPICAL CHARACTERISTICS



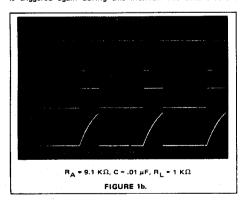
APPLICATIONS INFORMATION MONOSTABLE OPERATION

In this mode of operation, the timer functions as a oneshot. Referring to Figure 1a the external capacitor is initially held discharged by a transistor inside the timer.



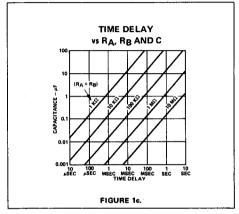
Upon application of a negative trigger pulse to pin 2, the flip-flop is set which releases the short circuit across the external capacitor and drives the output high. The voltage across the capacitor, now, increases exponentially with the time constant $\tau = R_AC$. When the voltage across the capacitor equals 2/3 VCC, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state. Figure 1b shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit will remain in this state until the set time is elapsed, even if it is triggered again during this interval. The time that the



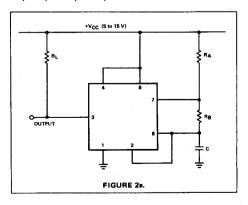
output is in the high state is given by $t = 1.1~R_AC$ and can easily be determined by Figure 1c. Notice that since the charge rate, and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse to the reset terminal (pin 4) during the timing cycle discharges the external capacitor and causes the cycle to start owner again. The timing cycle will now commence on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its low state.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.



ASTABLE OPERATION

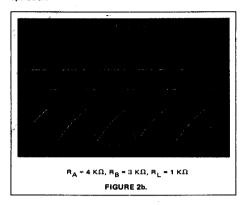
If the circuit is connected as shown in Figure 2a (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through RA and RB and discharges through RB only. Thus the duty cycle may be precisely set by the ratio of these two resistors.



APPLICATIONS INFORMATION (Cont'd)

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 2b shows actual waveforms generated in this mode of operation.



The charge time (output high) is given by:

$$t_1 = 0.685 (R_A + R_B) C$$

and the discharge time (output low) by:

$$t_2 = 0.685 (R_B) C$$

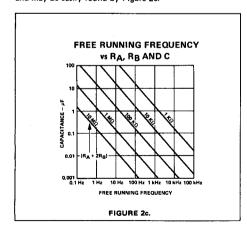
Thus the total period is given by:

$$T = t_1 + t_2 = 0.685 (R_A + 2R_B) C$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.46}{(R_A + 2R_B) C}$$

and may be easily found by Figure 2c.

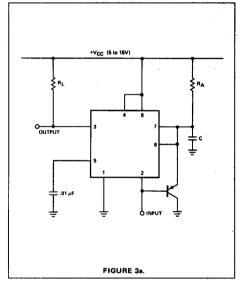


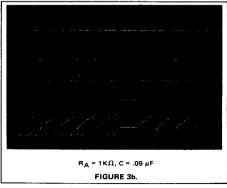
The duty cycle is given by:

$$D = \frac{R_B}{R_A + 2R_B}$$

MISSING PULSE DETECTOR

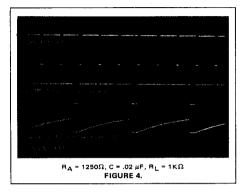
Using the circuit of Figure 3a, the timing cycle is continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows completion of the timing cycle which causes a change in the output level. For this application, the time delay should be set to be slightly longer than the normal time between pulses. Figure 3b shows the actual waveforms seen in this mode of operation.





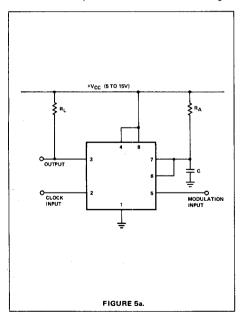
APPLICATIONS INFORMATION (Cont'd) FREQUENCY DIVIDER

If the input frequency is known, the timer can easily be used as a frequency divider by adjusting the length of the timing cycle. Figure 4 shows the waveforms of the timer in Figure 1a when used as a divide by three circuit. This application makes use of the fact that this circuit cannot be retriggered during the timing cycle.

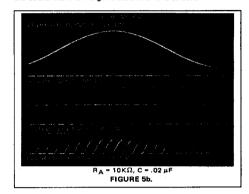


PULSE WIDTH MODULATION (PWM)

In this application, the timer is connected in the monostable mode as shown in Figure 5a. The circuit is triggered with a continuous pulse train and the threshold voltage is

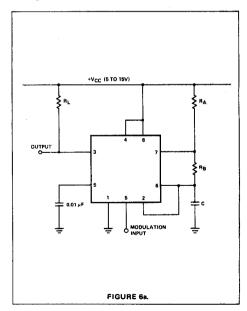


modulated by the signal applied to the control voltage terminal (pin 5). This has the effect of modulating the pulse width as the control voltage varies. Figure 5b shows the actual waveforms generated with this circuit.

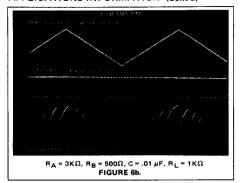


PULSE POSITION MODULATION (PPM)

This application uses the timer connected for astable (freerunning) operation, Figure 6a, with a modulating signal again applied to the control voltage terminal. Now the pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 6b shows the waveforms generated for triangle wave modulation signal.

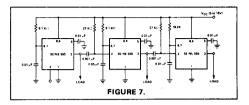


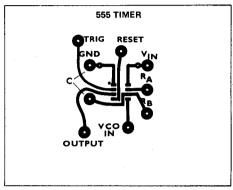
APPLICATIONS INFORMATION (Cont'd)



TEST SEQUENCER

Figure 7 shows several timers connected sequentially. The first timer is started by momentarily connecting pin 2 to ground, and runs for 10 msec. At the end of its timing cycle, it triggers the second circuit which runs for 50 msec. After this time, the third circuit is triggered. Note that the timing resistors and capacitors can be programmed digitally and that each circuit could easily trigger several other timers to start concurrent sequences.





PACKAGE INFORMATION

